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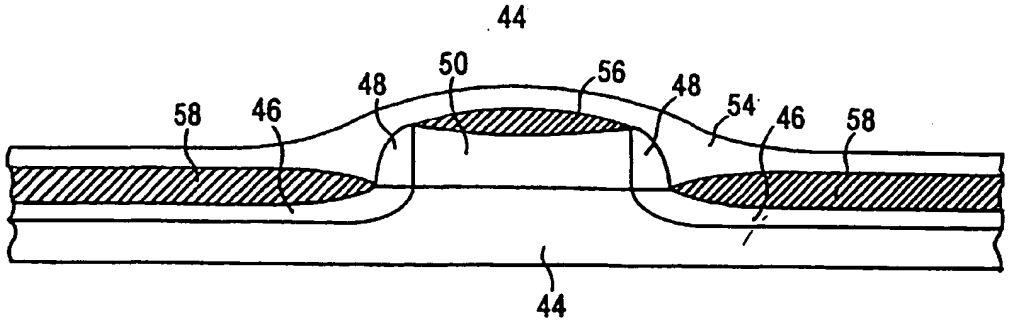
(54) Title: METHOD OF FORMING NICKEL SILICIDE USING A ONE-STEP RAPID THERMAL ANNEAL PROCESS AND BACKEND PROCESSING



(57) Abstract: A self-aligned silicide process that can accommodate a low thermal budget and form silicide regions (64, 66) of small dimensions in a controlled reaction. In a first temperature treatment, nickel metal or nickel alloy (52) is reacted with a silicon material (46) to form at least one high resistance nickel silicide region (56, 58). Unreacted nickel (54) is removed. A dielectric layer (60) is then deposited over the high resistance nickel silicide regions (56, 58). In a second temperature treatment, the at least one high resistance nickel silicide regions (56, 58) and dielectric (60) are reacted at a prescribed temperature to form at least one low resistance silicideregion (64, 66) and process the dielectri c layer (60). Bridging between regions is avoided by the two-step process as silicide growth is controlled, and unreacted nickel (54) between silicide region (56, 58) is removed after the first temperature treatment. The processing of the high resistance nickel silicide regions (56, 58) and the dielectric layer (60) are conveniently combined into a single temperature treatment. In other embodiments, the second temperature treatment is performed prior to, and separate from, the depositing and processing of the dielectric layer (60).

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METHOD OF FORMING NICKEL SILICIDE USING A ONE-STEP RAPID THERMAL ANNEAL PROCESS AND BACKEND PROCESSING

TECHNICAL FIELD

The present invention relates to a method of forming nickel silicide using a one step rapid thermal anneal and backend processing process.

BACKGROUND ART

Forming self-aligned silicides is well known in the semiconductor processing industry as a way of integrating low resistivity material on predefined regions of semiconductor structures that are being processed to form semiconductor devices. More specifically, self-aligned silicide processing is a method of reacting metal with silicon regions of a semiconductor structure to form silicide regions. Self-aligned silicides can be selectively formed on semiconductor structures without the necessity of patterning or etching the deposited silicide to define low resistively regions.

Titanium, cobalt, and nickel are among the metals that have been reacted with silicon materials to form self-aligned silicides on semiconductor structures. Titanium silicide can be formed on a semiconductor structure in a self-aligned manner. Figure 1 shows an exemplary silicon substrate 10 with a polycrystalline silicon region 16 formed on the silicon substrate 10. Adjacent to the polycrystalline silicon region 16 are spacers 14. The spacers 14 can be an oxide, nitride, or other ceramic material. The silicon substrate 10 has active regions 12 that can be characterized as being doped silicon and may function as the source and drain of a transistor. In Figure 2, a layer of titanium metal or titanium alloy 18 is deposited over the semiconductor structure of Figure 1. The semiconductor structure of Figure 2 then undergoes a first rapid thermal anneal (RTA) at temperatures ranging from 550°C to 750°C. Figure 3 shows the semiconductor structure of Figure 2 after this first rapid thermal anneal. Some of the titanium metal or titanium alloy layer 18 reacts with the polycrystalline region 16 to form high resistivity silicide ($TiSi_2$) regions 22. Additionally, some of the titanium layer 18 reacts with the silicon of the active region 12 to form high resistivity titanium silicide ($TiSi_2$) region 20. During the first rapid thermal anneal, none of the titanium layer 18 reacts with the spacer 14. As silicide does not form on the spacers, the high resistivity titanium silicide regions 20, 22 are formed in a self-aligned manner, as it is not necessary to pattern or etch silicide off the spacers to define the titanium silicide regions 20, 22 on the polycrystalline region 16 and active region 12. It is undesirable to form silicide on the spacers 14 as this leads to bridging between the gate and the source/drain 12. Unreacted titanium in metal layer 19 of Figure 3 is stripped away using conventional stripping techniques. Figure 4 shows the semiconductor structure of Figure 3 after the unreacted metal layer 19 is stripped away. The high resistivity titanium silicide regions 20, 22 remain integrated into the semiconductor structure after the wet strip of the unreacted metal 19. The semiconductor structure of Figure 4 then undergoes a second rapid thermal anneal at temperatures ranging from 750°C to 900°C. Figure 5 shows the semiconductor structure of Figure 4 after the second rapid thermal anneal where the high resistivity titanium silicide regions 20, 22 are reacted to form low resistivity silicide ($TiSi_2$) regions 24, 26. The low resistivity silicide titanium regions 24 are formed on the polycrystalline silicon region 16 and low resistivity titanium silicide regions 26 are formed on the active region 12 of the silicon substrate 10.

There are several disadvantages of the above described two-step rapid thermal anneal process using titanium metal or titanium alloy to form low resistivity titanium silicide in a self-aligned manner. As

semiconductor technology has advanced, it has become desirable for the dimensions of certain semiconductor structures to become smaller. For example, it is desirable for the polycrystalline region 16 and spacers 14 to be formed as small as possible on semiconductor substrate 10 to enhance performance of semiconductor devices using this type of structure. For example, transistors adopting this general semiconductor structure are designed and implemented with such small dimensions to enable the transistor to execute computer instructions at faster speeds. It is often necessary to form low resistivity titanium silicide regions on semiconductor structures to enable electrical interconnection of semiconductor components of a semiconductor device. Such exemplary regions are the active regions 12 and polycrystalline region 16 of Figure 5. The use of titanium in a two step rapid thermal anneal process to form titanium silicide in a self-aligned manner is not effective with semiconductor structures of smaller dimensions because titanium metal or titanium alloy layer does not fully react with the small surfaces of silicon materials such as the polycrystalline silicon region 16 and active regions 12 of Figures 1-5. The reasoning behind this shortcoming of titanium in a self-aligned silicide processes is that the reaction of titanium with silicon materials are dominated by nucleation of the silicide and therefore the silicide does not form in a consistent manner. As exemplified in Figures 3-5, the reaction of titanium metal or titanium alloy with the silicon materials forms titanium silicide regions that are scattered, inconsistent, and not adequate for the formation of silicide regions in some semiconductor devices, such as transistors. As not all of the titanium metal or titanium alloy reacts on the silicon material surfaces of small semiconductor structures, the reaction of titanium with the silicon based material does not adequately lower the resistivity of the silicon based components of the semiconductor structure. Hence, the use of titanium does not adequately serve the objectives of forming silicides in a self-aligned manner for relatively small semiconductor structures. This limitation of the use of titanium in self-aligned silicides is often referred to as line width dependence.

Another disadvantage of the use of titanium metal or titanium alloy to form titanium silicides in a semiconductor structure is that the temperatures at which the first and second rapid thermal anneal undergo are relatively high. These high temperatures limit the designs of the semiconductor structures utilizing self-aligned silicides. High temperatures can induce stress on the semiconductor structure and can destroy the functionality of the semiconductor device. Other disadvantages of a two-step rapid thermal anneal process to form titanium silicide are also known.

Cobalt can also be reacted with silicon materials, such as polycrystalline silicon or a silicon substrate, to form self-aligned cobalt silicide regions in a semiconductor structure. Figure 6, for example, shows a semiconductor substrate 10 with active regions 12 and a polycrystalline region 16 formed on the silicon substrate 10. Spacers 14 are formed on the silicon substrate 10 adjacent to the polycrystalline region 16. A layer of cobalt metal or cobalt alloy 28 is formed on the semiconductor structure of Figure 6, as shown in Figure 7. The semiconductor structure of Figure 7 undergoes a first rapid thermal anneal at temperatures ranging from 450°C to 510°C. Figure 8 shows high resistivity cobalt silicide (CoSi) regions 30, 32 formed on the polycrystalline region 16 and the active regions 12 as a product of the first rapid thermal anneal process. Any unreacted cobalt metal or cobalt alloy 29 is wet stripped away using conventional stripping techniques. Figure 9 shows the semiconductor structure of Figure 8 with high resistivity cobalt silicide 30, 32 regions formed on the polycrystalline region 16 and the active region 12 of the substrate 10 after unreacted cobalt metal or cobalt alloy 29 is stripped away. No cobalt silicide is formed on the spacers 14; this feature exemplifies the self-alignment characteristic of self-aligned silicides. Further, the stripping does not strip away any of the formed cobalt silicide

and only strips the unreacted cobalt metal or cobalt alloy 29. The semiconductor structure of Figure 9 then undergoes a second rapid thermal anneal at temperatures ranging from 760°C to 840°C. The second rapid thermal anneal reacts the high resistivity cobalt silicide regions 30, 32 to form low resistivity cobalt silicide ($CoSi_2$) regions 34, 36. Figure 10 shows low resistivity cobalt silicide regions 34, 36 formed on the polycrystalline silicon region and the active region 12 of the substrate 10.

There are several disadvantages of using cobalt metal or cobalt alloy reacted with silicon material to produce cobalt silicides in semiconductor processing. One disadvantage is that the two-step rapid thermal anneal process that is necessary to form low resistivity $CoSi_2$ require relatively high temperatures. These relatively high temperatures may not be compatible or desirable with semiconductor processing of pre-existing components of the semiconductor structure. More particularly, these high temperatures may induce stress on other semiconductor components and/or diffuse materials of the existing semiconductor structure.

The use of nickel to form self-aligned silicides has been established using a one-step rapid thermal anneal process. Figure 11, for example, shows a silicon substrate 10 with active regions 12. A polycrystalline silicon region 16 is formed on the silicon substrate 10 and spacers 14 are formed adjacent to the polycrystalline silicon region 16. A layer of nickel metal or nickel alloy is formed on the exemplary semiconductor structure of Figure 11. Figure 12, for example, shows a layer of nickel metal or nickel alloy 38 formed over the semiconductor structure of Figure 11. A single rapid thermal anneal is conducted at temperatures ranging from 350°C to 700°C in order to react the nickel metal or nickel alloy to form a silicide with a relatively low resistance. Figure 13, for example, depicts silicide regions 40, 42 formed from the single rapid thermal anneal. At the necessary rapid thermal anneal temperatures ranging from 350°C to 700°C, undesirable bridging may occur between the nickel silicide formed on polycrystalline silicon region 16 and the nickel silicide formed on the active regions 12. The unreacted nickel in layer 4A is stripped, leaving the structure of Figure 14.

There are certain concerns arising from the one-step rapid thermal anneal of nickel silicide. One concern is the relatively uncontrollable reaction and excessive formation of nickel silicide, which may cause the aforementioned bridging between the nickel silicide 40 formed on the polycrystalline silicon 16 and the nickel silicide 42 formed on the active regions 12, as seen in Figure 14.

DISCLOSURE OF THE INVENTION

There is a need for a self-aligned silicide process that can accommodate a low thermal budget during processing and with a controlled silicidization reaction of metal or alloy with silicon material. Further, there is a need for a self-aligned silicide process that can combine processing steps during the fabrication of semiconductor devices.

These and other needs are met by embodiments of the present invention which provide a one-step temperature treatment process and backend processing to form self-aligned nickel silicide regions in a semiconductor structure. The present invention includes depositing a layer of nickel metal or nickel alloy on silicon material. At least a section of the nickel metal or alloy is reacted with at least a section of the silicon layer at a first temperature for a first period of time to form at least one high resistance nickel silicide layer. Unreacted nickel metal or nickel alloy is removed from the semiconductor structure leaving the at least one high resistance silicide layer integrated into the semiconductor structure. A dielectric layer is then deposited over the at least one high resistance nickel silicide layer. The dielectric layer and the at least one high resistance nickel silicide layer undergo a second temperature for a second period of time to form at least one low resistance nickel silicide layer.

The present invention has the advantage of producing silicide at a relatively low temperature. This feature reduces stress on other pre-existing semiconductor components of a semiconductor structure. This feature also allows the semiconductor processing of more complicated and useful semiconductor structures. Another advantage of the present invention is that the nickel metal layers react with the silicon based material layers in a controlled manner. This is an important and useful attribute as enough nickel silicide is reacted such that line width dependence is not an obstacle and bridging between silicide regions formed on the same semiconductor structure is prevented. Further, the present invention has the advantage of combining the processing of the high resistance nickel silicide layer and processing of the dielectric layer in a single step of undergoing a second temperature for a second period of time.

The earlier stated needs are also met by embodiments of the present invention which provide a two-step temperature treatment process to form self-aligned nickel silicide regions in a semiconductor structure. The two-step temperature treatment includes depositing a layer of nickel metal or nickel alloy on silicon material. At least a section of the nickel metal or alloy is reacted with at least a section of the silicon layer at a first temperature for a first period of time to form at least one high resistance nickel silicide layer. All unreacted nickel metal or nickel alloy is removed from the semiconductor structure leaving the at least one high resistance silicide layer integrated into the semiconductor structure. The at least one high resistance nickel silicide layer is reacted at a second temperature for a second period of time to form at least one low resistance nickel silicide layer.

The present invention has the advantage of producing silicide at a relatively low temperature. This feature reduces stress on other pre-existing semiconductor components of a semiconductor structure. This feature allows the semiconductor processing of more complicated and useful semiconductor structures. Another advantage of the present invention is that the nickel metal layers react with the silicon based material layers in a controlled manner. This is an important and useful attribute as enough nickel silicide is reacted such that line width dependence is not an obstacle and bridging between silicide regions formed on the same semiconductor structure is prevented.

The foregoing and other features, aspects, and advantages of the present invention will become more apparent from the following detailed description of the present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a prior art diagram of a typical semiconductor structure prior to the formation of a silicide.

Figure 2 is a prior art diagram of the semiconductor structure of Figure 1 with a titanium metal or titanium alloy layer deposited on the semiconductor structure.

Figure 3 is a prior art diagram of the semiconductor structure of Figure 2 after a first rapid thermal anneal.

Figure 4 is a prior art diagram of the semiconductor structure of Figure 3 after the removal of unreacted titanium metal or titanium alloy.

Figure 5 is a prior art diagram of the semiconductor structure of Figure 4 after a second rapid thermal anneal.

Figure 6 is a prior art diagram of a typical semiconductor structure prior to the formation of a silicide.

Figure 7 is a prior art diagram of the semiconductor structure of Figure 6 with a layer of cobalt metal or cobalt alloy deposited on the semiconductor structure.

Figure 8 is a prior art diagram of the semiconductor structure of Figure 7 after a first rapid thermal anneal.

Figure 9 is a prior art diagram of the semiconductor structure of Figure 8 after the unreacted cobalt metal or cobalt alloy is stripped away.

Figure 10 is a prior art diagram of the semiconductor structure of Figure 9 after a second rapid thermal anneal.

Figure 11 is a prior art diagram of a typical semiconductor structure prior to the formation of a silicide.

Figure 12 is a prior art diagram of the semiconductor structure of Figure 11 after a layer of nickel metal or nickel alloy is deposited on the semiconductor structure.

Figure 13 is a prior art diagram of the semiconductor structure of Figure 12 after a single rapid thermal anneal.

Figure 14 is a prior art diagram of the semiconductor structure of Figure 13 after the unreacted nickel metal or nickel alloy has been stripped away.

Figure 15 is a diagram of a semiconductor structure.

Figure 16 is a diagram of the semiconductor structure of Figure 15 with a layer of nickel metal or nickel alloy deposited on the semiconductor structure.

Figure 17 is a diagram of the semiconductor structure of Figure 16 after a first temperature treatment.

Figure 18 is a diagram of the semiconductor structure of Figure 17 after the unreacted nickel metal or nickel alloy has been stripped away.

Figure 19 is a diagram of the semiconductor structure of Figure 18 after the deposition of a dielectric layer.

Figure 20 is a diagram of a semiconductor structure of Figure 19 after a second temperature treatment.

MODE(S) FOR CARRYING OUT THE INVENTION

The present invention relates to a one-step temperature treatment and backend processing for forming nickel silicide on a semiconductor structure. The process of the present invention includes depositing a nickel metal or nickel alloy on a silicon layer. The nickel metal or nickel alloy and the silicon layer are reacted at a first temperature for a first period of time to form at least one high resistance nickel silicide region. The unreacted nickel metal or nickel alloy is then stripped away and at least one high resistance nickel silicide region remains integrated into the semiconductor structure. A dielectric layer is then deposited over the higher resistance nickel silicide regions. The at least one high resistance nickel silicide region and dielectric layer undergo a second temperature for a second period of time to form at least one low resistance nickel silicide region. By employing a one-step temperature treatment and backend processing process, instead of a single step rapid thermal anneal process typically employed in turning nickel silicide, the present invention mitigates bridging between silicide regions of a semiconductor device and reduces the number of steps necessary to process a given semiconductor device. In other embodiments of the invention, the second annealing step is performed prior to deposition of the dielectric layer, to form the lower resistance nickel silicide regions.

Figure 15 is an exemplary semiconductor structure. The semiconductor structure includes a silicon substrate 44 with a polycrystalline silicon region 50 formed on the silicon substrate 44. Adjacent to the polycrystalline region 50 are spacers 48. The silicon substrate 44 may also include active regions. The active regions may be characterized by doped silicon. The polycrystalline region 50 formed on the silicon substrate 44

may serve as a gate for a transistor and the active regions 46 may serve as the source and the drain for a transistor. The spacers 48 may be formed from an oxide, nitride, or other ceramic material. The function of the spacers 48 may be to isolate the polycrystalline region 50 from the active regions 46 or to isolate the gate of a transistor from the source and drain of a transistor.

Figure 16 shows the semiconductor structure of Figure 15 after nickel metal or nickel alloy 52 has been deposited in a conventional manner on the semiconductor structure. Figure 17 depicts the semiconductor structure of Figure 16 after a first temperature treatment that reacts the nickel metal or nickel alloy 52 with the polycrystalline region 50 and active regions 46 to form high resistivity nickel silicide (Ni_3Si or Ni_2Si) regions 56. The first temperature treatment is at temperatures ranging from 250°C to 350°C. This temperature treatment is at a relatively low temperature compared to the single step rapid thermal anneal temperatures of the prior art employed to create nickel silicide, or to the temperature employed in the first rapid thermal anneal of prior art titanium silicide or prior art cobalt silicide. Further, the first temperature treatment can be a rapid thermal anneal characterized by fast ramp up and fast ramp down of the temperature over a relatively short period of time. Exemplary annealing processes that can be used for the rapid thermal anneal are a laser annealing process, a lamp heated annealing process, or other radiative annealing process. The first temperature treatment may be for a first period of time ranging from 15 seconds to 90 seconds, but preferably for 30 seconds to 60 seconds.

In Figure 18, the semiconductor structure of Figure 17 is stripped of unreacted nickel metal or nickel alloy 54 by a conventional stripping technique. Exemplary conventional stripping techniques include use of a sulfuric peroxide, hydrochloric acid, nitric acid, phosphoric acid, or mixtures of these stripping agents. The stripping of the unreacted nickel metal or nickel alloy 54 does not remove the relatively high resistance nickel silicide regions 56, 58 formed in the first temperature treatment. Further, none of the nickel metal or nickel alloy 52 is reacted on the spacers 48, as the spacers are formed of an oxide or nitride or other such material. The low temperature used in this stage of nickel silicide formation prevents uncontrolled silicide formation on the spacers 48, in contrast to what can occur in a typical single step nickel silicide formation process. This feature serves the function of self-alignment, as it is not necessary for the nickel silicide areas to be etched in order to isolate nickel silicide regions 56, 58 at the desirable locations on the semiconductor structure.

Figure 19 is a depiction of a dielectric layer deposited over the semiconductor structure of Figure 18. The dielectric layer 60 is a further component of the semiconductor structure and may be unrelated to the formation of silicide in the semiconductor structure. Dielectric layer 60 may serve as an isolation layer prior to processing through a temperature treatment.

Figure 20 is a depiction of the semiconductor structure of Figure 19 after a second temperature treatment in accordance with an exemplary embodiment of the present invention. The second temperature treatment is at temperatures ranging from 350°C to 700°C. Further, the second heat treatment can be a rapid thermal anneal characterized by a fast ramp up and ramp down to the target temperature of the temperature treatment. The high resistance nickel silicide regions of the embodiment of Figure 18 are reacted ("transformed") to form low resistance nickel silicide regions (NiSi) 52, 54. Further, the second temperature treatment also serves to process dielectric layer 60 of Figure 19 to layer 62 of Figure 20. The processing of silicide regions 56, 58 and dielectric layer 60 is backend processing. Backend processing is a term of art used to describe a process step accomplished in a subsequent process step. In certain preferred embodiments, the second temperature treatment is at temperatures ranging from about 350°C to about 700°C in order to form the lowest resistivity nickel silicide

and maintain a reasonable low thermal budget. The second temperature treatment is a relatively low temperature compared to the rapid thermal anneal temperatures required by the prior art for other types of silicides. The time period for the second temperature treatment can be between 15 seconds and 15 minutes.

In alternative embodiments, the second temperature treatment is performed prior to the depositing of the dielectric layer 60, and hence, forms the lower resistance nickel silicide before, and separate from, the continued backend processing.

The present invention offers a self-aligned silicide process that can accommodate a low thermal budget and form silicide regions of small dimensions in a controlled reaction. The present invention achieves this through a one-step temperature treatment forming high resistance nickel silicide and backend processing to process a dielectric layer and form low resistance nickel silicide from the high resistance nickel silicide. In a first temperature treatment, nickel metal or nickel alloy is reacted with a silicon material to form high resistance nickel silicide regions unreacted metal or nickel alloy is then stripped from the semiconductor structure. A dielectric layer is then deposited over the high resistance nickel silicide regions. In a second temperature treatment, the high resistance nickel silicide regions are reacted at a prescribed temperature to form low resistance silicide regions and at the same time the dielectric layer is processed. The use of a two-step temperature treatment allows for the formation of silicide of small dimensions in a controlled manner and at a relatively low temperature. The present invention can effectively form silicide and accommodate a low thermal budget during semiconductor processing while, largely avoiding the bridging exhibited by prior art techniques of forming nickel silicide. Further, the present invention can combine the processing of the dielectric layer and the high resistance silicide region in the same temperature treatment step.

Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustrating and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

CLAIMS

WHAT IS CLAIMED IS

1. A semiconductor processing process, comprising the steps of:

depositing nickel metal or nickel alloy (52) on at least one silicon layer (46);

reacting at least a portion of the nickel metal or nickel alloy (52) with the silicon layer (46) at a first temperature for a first period of time to form at least one high resistance nickel silicide region (56, 58);

removing unreacted nickel metal or nickel alloy (54); and

reacting the high resistance nickel silicide region (56, 58) at a second temperature for a second period of time to form at least one low resistance nickel silicide region (64, 66).

2. The semiconductor processing process of claim 1, further comprising depositing a dielectric layer (60) over at least one high resistance nickel silicide region (56 58) prior to reacting the high resistance nickel silicide region (56, 58).

3. The semiconductor processing process of claim 1, wherein the first temperature is in the range of about 250°C to about 350°C.

4. The semiconductor processing process of claim 1, wherein the second temperature is in the range of about 400°C to about 600°C.

5. The semiconductor processing process of claim 1, wherein the high resistance nickel silicide region (56, 58) is at least one of Ni_3Si and Ni_2Si and the low resistance nickel silicide region (64, 66) is NiSi.

6. The semiconductor processing process of claim 1, wherein the first period of time is about 15 to about 90 seconds and the second period of time is about 15 to about 90 seconds.

7. The semiconductor processing process of claim 1, wherein the first period of time is about 30 to about 60 seconds and the second period of time is about 30 to about 60 seconds.

8. The semiconductor processing process of claim 1, wherein the first and second reacting steps form a two-step rapid thermal anneal process.

9. The semiconductor processing process of claim 2, wherein the first reacting step and the second reacting step from a one-step rapid thermal anneal with backend processing process.

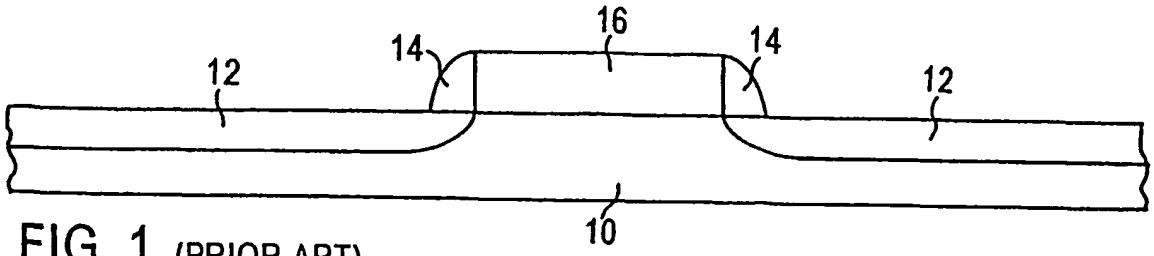

FIG. 1 (PRIOR ART)

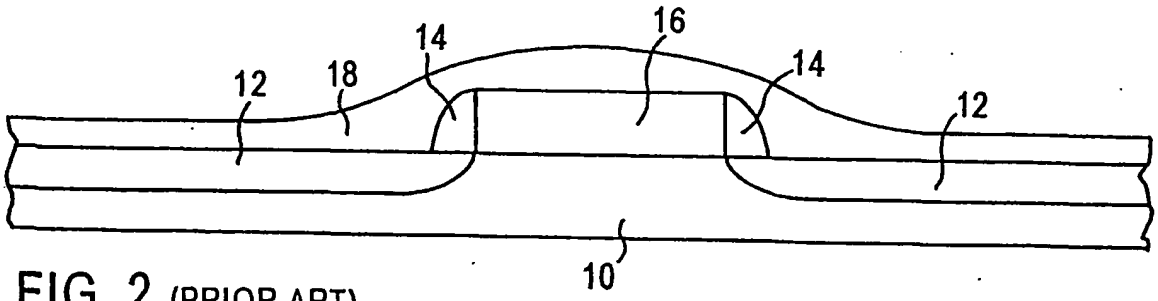

FIG. 2 (PRIOR ART)

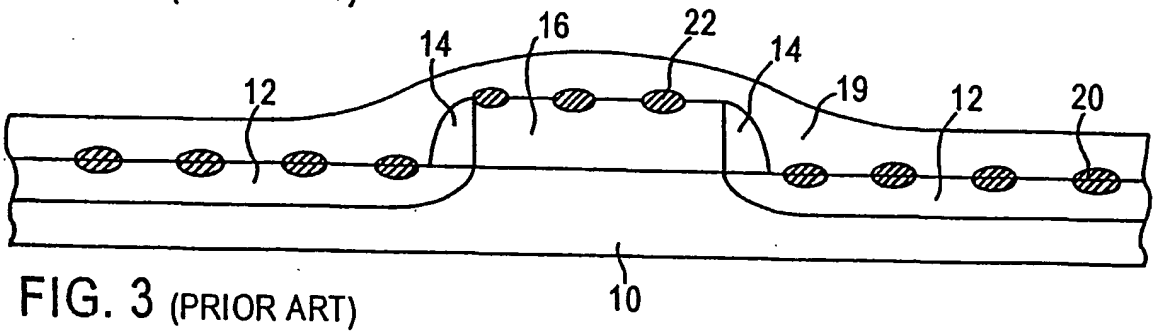

FIG. 3 (PRIOR ART)

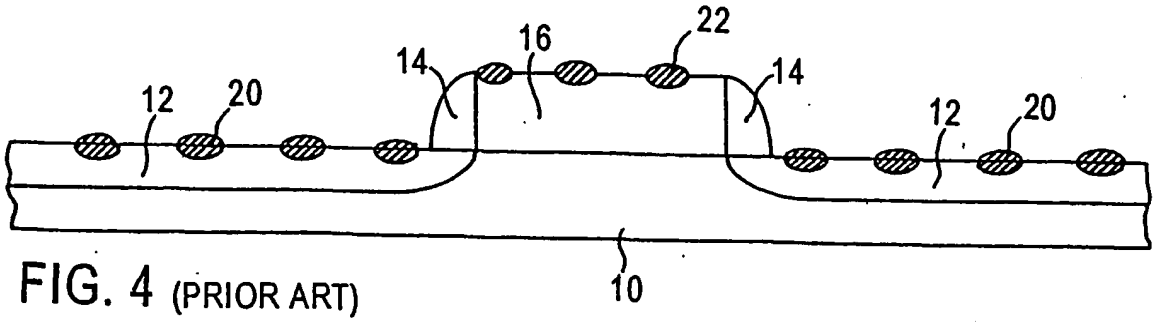

FIG. 4 (PRIOR ART)

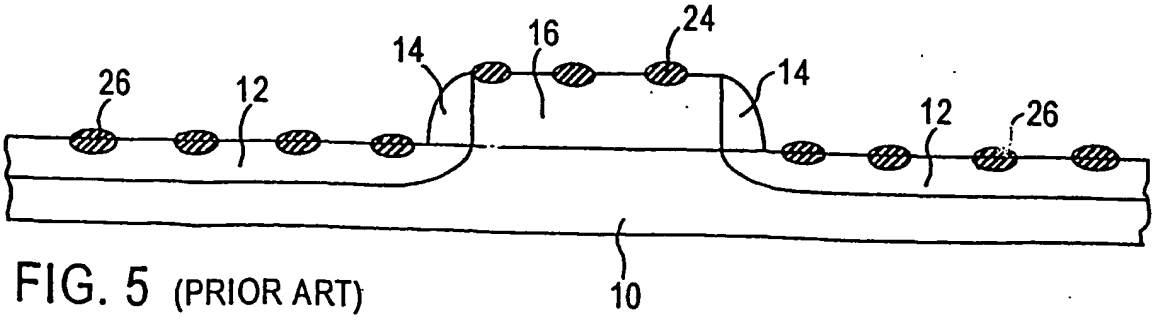

FIG. 5 (PRIOR ART)

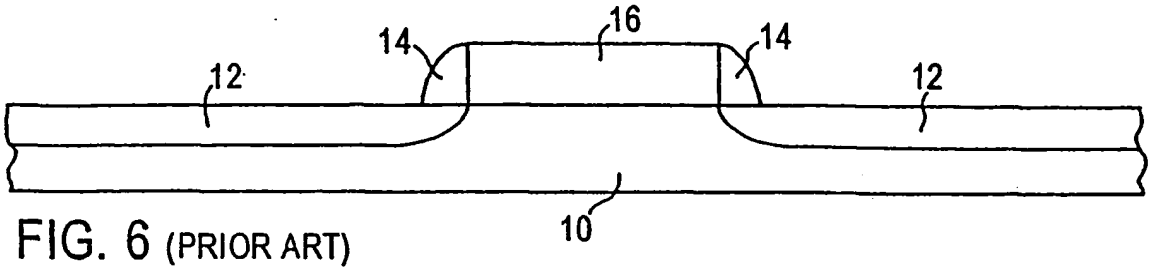

FIG. 6 (PRIOR ART)

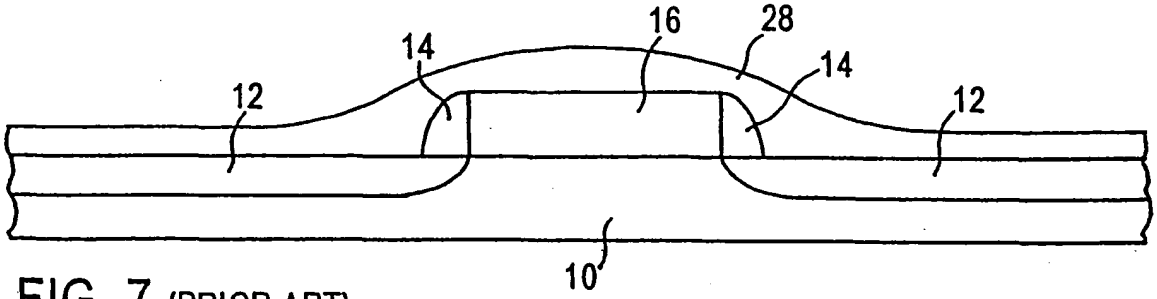

FIG. 7 (PRIOR ART)

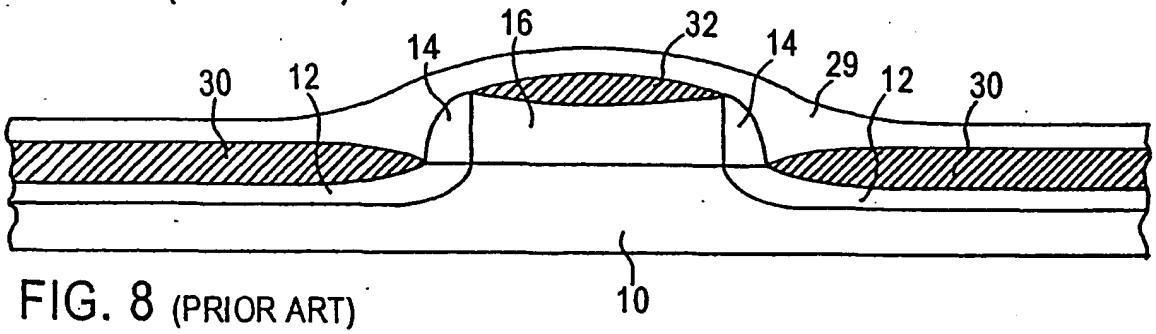

FIG. 8 (PRIOR ART)

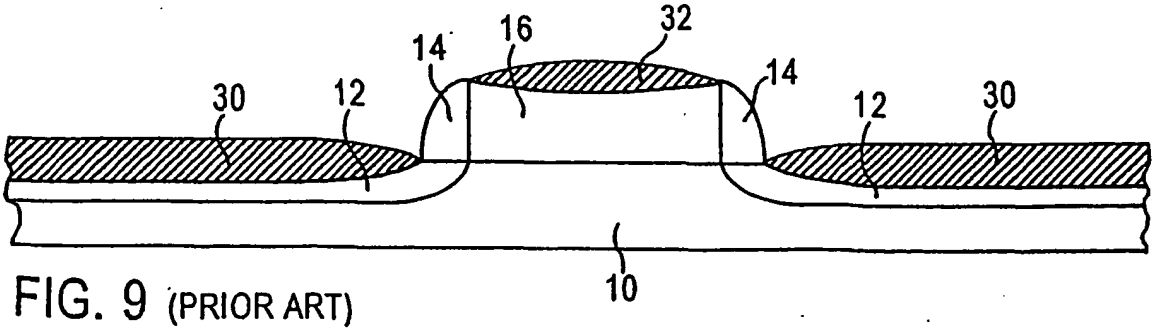

FIG. 9 (PRIOR ART)

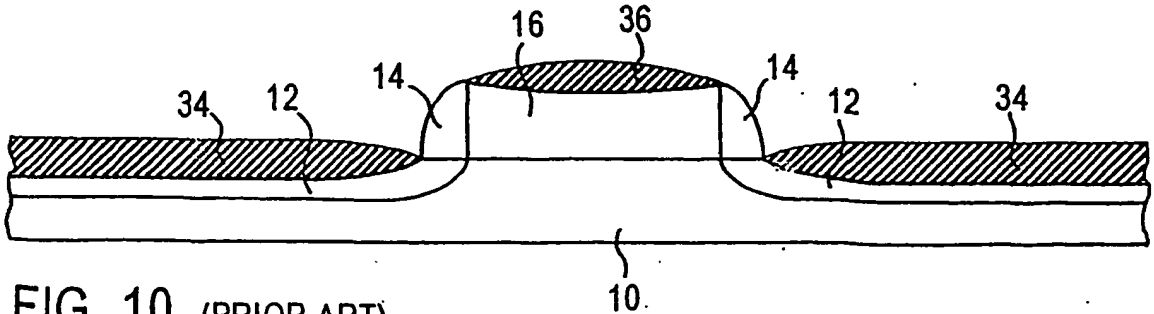

FIG. 10 (PRIOR ART)

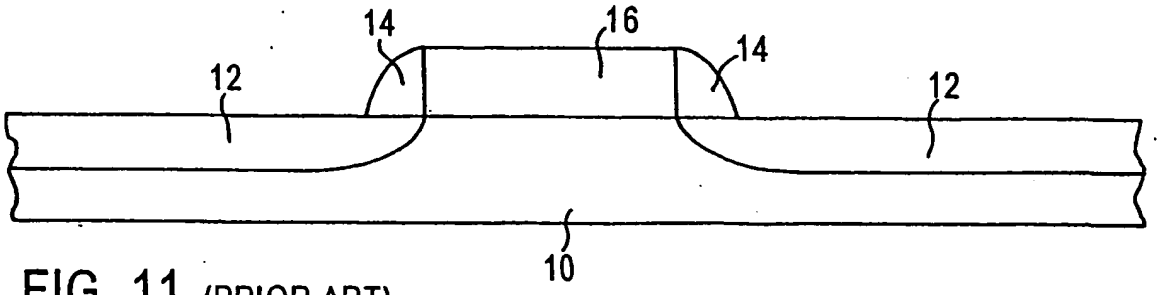

FIG. 11 (PRIOR ART)

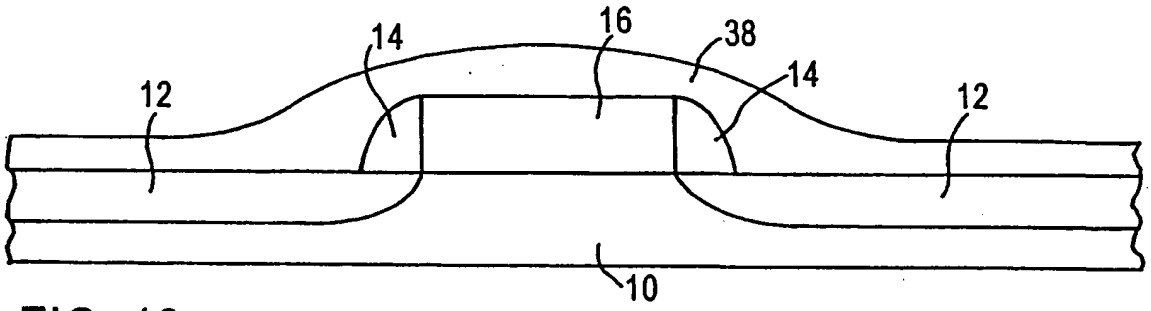

FIG. 12 (PRIOR ART)

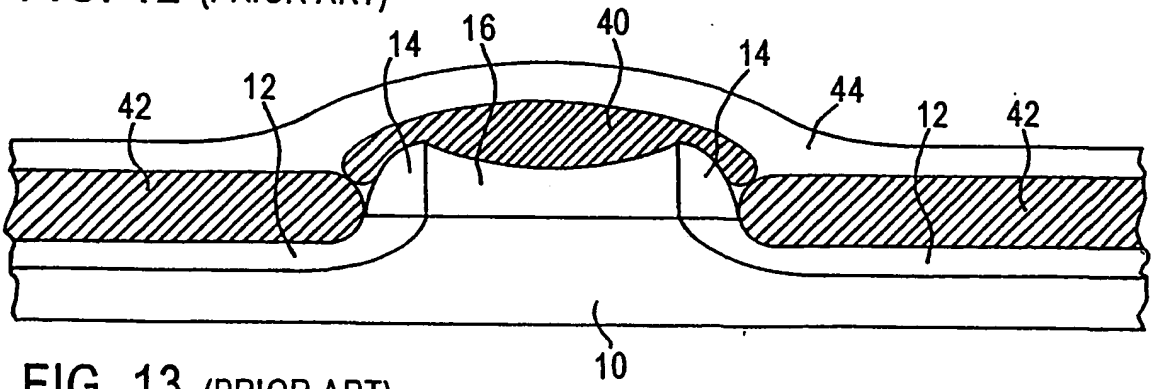

FIG. 13 (PRIOR ART)

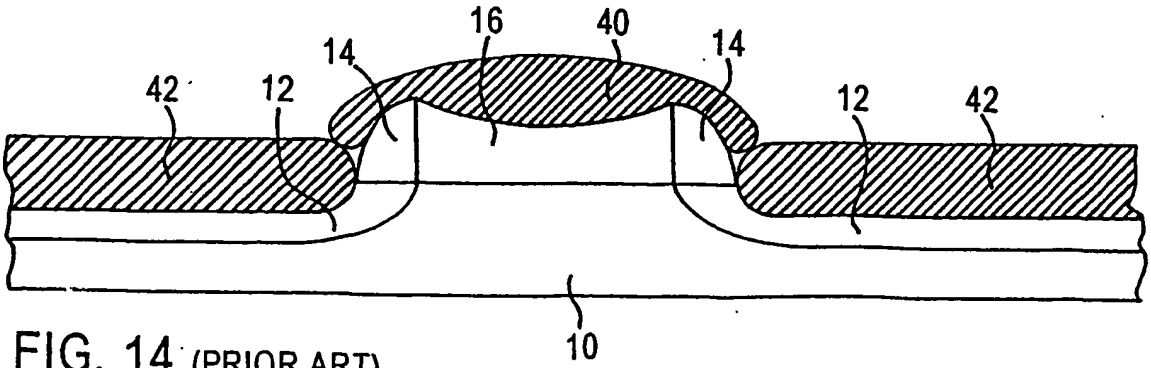

FIG. 14 (PRIOR ART)

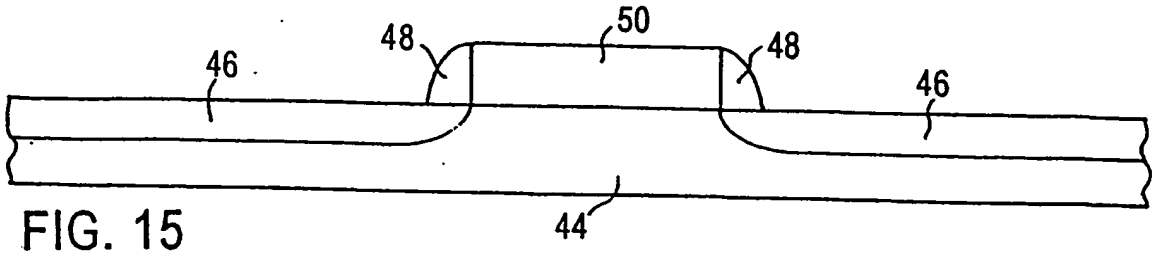

FIG. 15

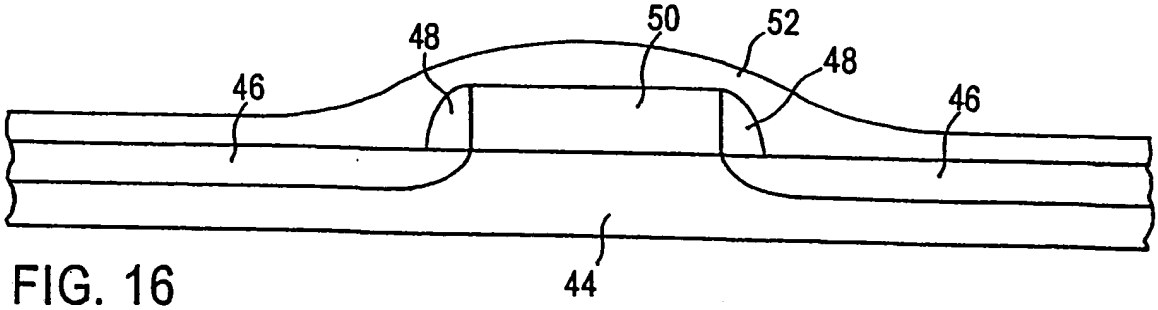

FIG. 16

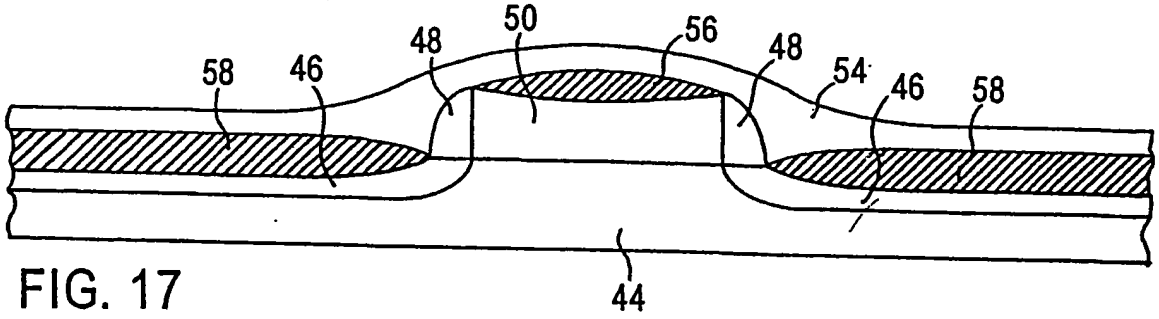

FIG. 17

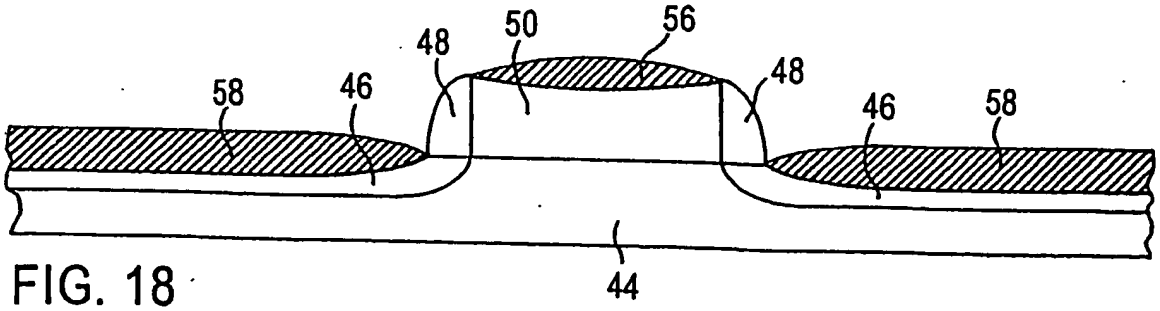

FIG. 18

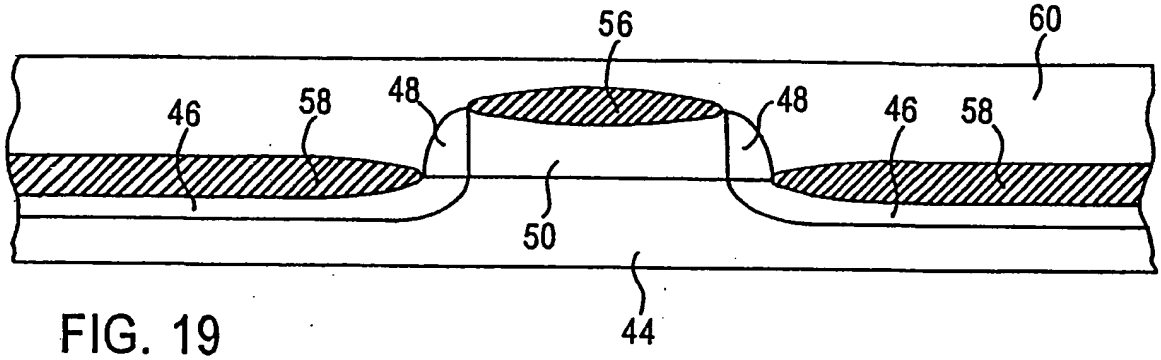

FIG. 19

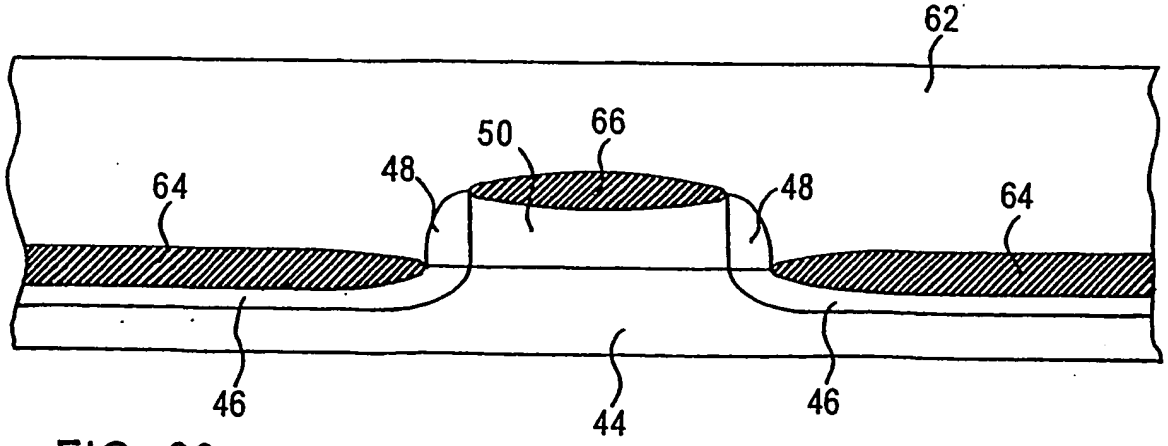

FIG. 20

INTERNATIONAL SEARCH REPORT

Ir tional Application No
PCT/US 01/45829

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP 0 936 664 A (SHARP KK ;SHARP MICROELECT TECH INC (US)) 18 August 1999 (1999-08-18) column 6, line 15 - line 48; figures 6,7 column 7, line 9 - line 32; figures 8,9 figure 15	1,3-6,8 2,9
Y	EP 0 831 521 A (TEXAS INSTRUMENTS INC) 25 March 1998 (1998-03-25) page 5, line 54 - line 48; figures 3B-3G	2,9
A	EP 0 836 223 A (TEXAS INSTRUMENTS INC) 15 April 1998 (1998-04-15) page 4, column 6, line 28 - line 31; figures 3A-3F	2,9
A	US 5 953 612 A (LIN XI-WEI ET AL) 14 September 1999 (1999-09-14) the whole document	1-9

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Date of the actual completion of the international search	Date of mailing of the international search report
11 April 2002	18/04/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nesso, S

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INTERNATIONAL SEARCH REPORT

Information on patent family members

li ational Application No
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